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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/697,503	10/30/2003	David A. Luick	ROC920020009US1	8053

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EXAMINER	
YU, JAE UN	

ART UNIT	PAPER NUMBER
2185	

DATE MAILED: 01/20/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/697,503	LUICK, DAVID A.	
	Examiner	Art Unit	
	Jae U. Yu	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

The instant application having Application No. 10697503 has a total of 16 claims pending in the application, there are 3 independent claims and 13 dependent claims, all of which are ready for examination by the examiner.

Oath/Declaration

The applicant's oath/declaration has been reviewed by the examiner and is found to conform to the requirements prescribed in 37 C.F.R. 1.63.

Drawings

The applicant's drawings submitted on 10/30/2003 are acceptable for examination purposes.

Specification

There is a spelling error in paragraph 25, at line 2. The word "sown" should be replaced with "shown".

Claim Rejections - 35 USC § 112 – 1st

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

1. **Claim 15** is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor, at the time the application was filed, had possession of the claimed invention.

Claim 15 is a means plus function claim, and interpreted according to 35 U.S.C. 112 sixth paragraph. The "means for pipelining one or more data loads" and the "means for selectively flagging one or more data loads to indicate dependence upon the load of a specific data load" do not appear to be disclosed in the instant specification.

Claim Rejections - 35 USC § 112 – 2nd

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

1. Claims 14-16 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

2. **Claim 14** recites, "The method of claim 7." However, claim 7 is an apparatus claim and it appears that it should depend on the method of claim 9 instead.

3. **Claim 16** recites, "The system of claim 13." However, claim 13 is a method claim and it appears that should depend on the system of claim 15 instead.

4. **Claim 15** is a means plus function claim, and interpreted according to 35 U.S.C. 112 sixth paragraph.

The claim appears to be indefinite since it is unclear whether the "one or more data loads" referred to in line 7 are the same "one or more data" loads" referred to in line 3 of claim 15. If the "one of more data loads" are the same then the applicant should insert the word, "the" or "said" in line 7 after the word "loading".

The "means for pipelining one or more data loads" and the "means for selectively flagging one or more data loads to indicate dependence upon the load of a specific data load" are not disclosed in the specification in a manner which one skilled in the art would be able to identify the structure from the description in the instant specification for performing the recited function. See MPEP 2181 (III). Accordingly, the limitation is indefinite.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. Claims 1-6 and 9-14 are rejected under 35 U.S.C. 103 (a) as being obvious over Peir et al. (US 2003/0208665 A1) in view of Au (US 5,548,795).

2. As per independent **claim 1,** "One or more pipelines **[Paragraph 11, Lines 2-3]**, each pipeline able to load **[Paragraph 11, Lines 2-3]**, execute **[Paragraph 12, Lines 3-8]**, and flush **[the instruction cancellation in Paragraph 12, Lines 3-4]** a series of data load."

"At least one fast-load data cache that loads one or more speculative data loads." **Peir et al. discloses the cache (110) in Figure 1, and the "cache hit" determination step in Figure 3**. If there is a cache hit, data must, inherently, have been loaded into the cache.

"Wherein upon determination of a misprediction for a specific speculative data load, the data loads flagged as dependent on that specific speculative data load not being executed in the one or more pipelines." **In Figure 3, Peir et al. discloses the "cache hit/miss" determination step.** The cache miss corresponds to the "misprediction" from the claim. If cache miss is detected, **"Cancel instructions scheduled during speculative window (330, Fig. 3)."** The "speculative window" corresponds to the data loads that are dependent on the speculative data load from the claim.

Peir et al. discloses keeping track of speculative load dependency, as disclosed above. However, Peir et al. does not disclose expressly the limitation, "the data loads flagged as dependent on that specific speculative load".

Au discloses, "Each data load selectively flagged to indicate dependence upon the loading of a specific data load". **"The D_Flag fields 308 in each record 202 indicate dependency relative to a more forward command record 202" in column 8, at lines 44-46 and in Figure 3.**

Peir et al. and Au are analogous art because they are from the same field of endeavor of determining and processing data/instructions that are dependent on other data/instructions.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify Peir et al. by including the step of setting a flag bit as taught by Au in column 8, at lines 44-46.

The motivation for doing so would have been to "maintain all command dependencies in a graph structure to reduce the number of address overlap-checks required" as expressly taught by Au in column 7, at lines 14-15.

Therefore, it would have been obvious to combine Au with Peir et al. for the benefit of command dependency indication to obtain the invention as specified in claim 1.

3. As per **claim 2**, "The speculative data load is loaded in the one or more pipelines." **Peir et al. discloses, "The processor 100 may establish a cache hit/miss prediction table (CPT) to record the hit/miss history of memory**

references and use the CPT to predict cache hit/miss for future memory reference" in paragraph 13. The "processor" corresponds to the "pipelines" from the claim, and the "CPT" corresponds to the "speculative data" from the claim.

4. As per **claim 3**, "one or more of the data loads in the one or more pipelines are not dependent on any specific data load and not selectively flagged." **Peir et al. discloses, "Independent instructions scheduled during this one cycle window may be allowed to continue regardless" in paragraph 16.** Independent instructions ("the data loads that are not dependent" from the claim) are always executed and flagging them is inherently unnecessary.

5. As per **claim 4**, Peir et al. and Au disclose the system recited in claim 1.

Au discloses, in **Figure 3**, the "D_Flag" field 308 within "Command Record" 202. Record 202 corresponds to the "data load" from the claim. The "D_Flag" is a bit since it represents a bistate field **(Column 7, Lines 46-48).**

6. As per **claim 5**, Peir et al. and Au disclose the system recited in claim 1.

Au discloses, in **Figure 3,** the "D_Flag" field 308 attached to the "Logical Block Address" 302 and 304. The "Logical Block Addresses" correspond to the "data load" from the claim. In addition, examiner notes that mere separation of parts (i.e. flags and data load) is not a patentable distinction over the prior art. See MPEP 2144.04 (C).

7. As per **claim 6**, the limitation, "the flagged dependent specific data load is flushed from the one or more pipelines upon the determination of a misprediction for a data load" is disclosed.

Peir et al. discloses **"A cache miss is detected during the regular cache access, all of the instructions that are scheduled during the speculative window may be canceled" in paragraph 18 and in Figure 3 (330).** The "flushing" from the claim corresponds to the instruction cancellation, and the "misprediction" from the claim corresponds to the "cache miss".

Peir et al. does not disclose expressly the limitation "flagged dependent specific data load".

Au discloses **"The D_Flag fields 308 in each record 202 indicate dependency relative to a more forward command record 202" in Figure 3 and in column 8, at lines 44-46.**

Peir et al. and Au are analogous art because they are from the same field of endeavor of determining and processing data/instructions that are dependent on other data/instructions.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify Peir et al. by including the step of setting a flag bit as taught by Au in column 8, at lines 44-46.

The motivation for doing so would have been to "maintain all command dependencies in a graph structure to reduce the number of address overlap-checks required" as expressly taught by Au in column 7, at lines 14-15.

Therefore, it would have been obvious to combine Au with Peir et al. for the benefit of command dependency indication to obtain the invention as specified in claim 6.

8. As per independent **claim 9**, "loading one or more data into a pipeline." **Peir et al. recites, "A deeply pipelined, load/store architecture" in paragraph 11.**

"Loading a speculative data load in a fast-load data cache." **In Figure 3, Peir et al. discloses the "cache hit" determination step.** If there is a cache hit, data must, inherently, have been loaded into the cache.

"Determining if the speculative data load is a misprediction." **In Figure 3, Peir et al. discloses the "cache hit" determination step.** The cache miss ("No" from the determination step) corresponds to the data misprediction from the claim.

"Selectively executing the data loads not flagged as dependent on that specific data load determined to be misprediction". The examiner's interpretation is that independent data loads ("not flagged as dependent") are executed even if there is a cache miss (misprediction). **Peir et al. recites, "If the entry indicates a miss, the dependent instructions my be canceled and recovered in the next cycle. Independent instructions scheduled during this one cycle window may be allowed to continue regardless" in paragraph 16.**

Peir et al. does not disclose expressly the limitation "selectively flagging one or more data loads to indicate dependence upon the load of a specific data load". **Au recites, "The D_Flag fields 308 in each record 202 indicate dependency relative to a more forward command record 202" in column 8, at lines 44-46 and in Figure 3.**

Peir et al. and Au are analogous art because they are from the same field of endeavor of determining and processing data/instructions that are dependent on other data/instructions.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify Peir et al. by including the step of setting a flag bit as taught by Au in column 8, at lines 44-46.

The motivation for doing so would have been to "maintain all command dependencies in a graph structure to reduce the number of address overlap-checks required" as expressly taught by Au in column 7, at lines 14-15.

Therefore, it would have been obvious to combine Au with Peir et al. for the benefit of command dependency indication to obtain the invention as specified in claim 9.

9. As per **claim 10**, the limitation "loading the speculative data load into the pipeline" is disclosed. **Peir et al. discloses, "The processor 100 may establish a cache hit/miss prediction table (CPT) to record the hit/miss history of memory references and use the CPT to predict cache hit/miss for future memory**

reference" in paragraph 13. The "processor" corresponds to the "pipelines" from the claim, and the "CPT" corresponds to the "speculative data" from the claim.

Peir et al. does not disclose expressly the flagging concept recited in claim 9. However, Au discloses the flagging concept that is used to reject claim 9.

Peir et al. and Au are analogous art because they are from the same field of endeavor of determining and processing data/instructions that are dependent on other data/instructions.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify Peir et al. by including the step of setting a flag bit as taught by Au in column 8, at lines 44-46.

The motivation for doing so would have been to "maintain all command dependencies in a graph structure to reduce the number of address overlap-checks required" as expressly taught by Au in column 7, at lines 14-15.

Therefore, it would have been obvious to combine Au with Peir et al. for the benefit of command dependency indication to obtain the invention as specified in claim 10.

10. As per **claim 11**, the limitation "does not flag any data load that is not dependent on any specific data load" is disclosed. **Peir et al. discloses, "Independent instructions scheduled during this one cycle window may be allowed to continue regardless" in paragraph 16.** Independent instructions ("the data loads that are not

dependent" from the claim) are always executed and flagging them is inherently unnecessary.

Peir et al. does not disclose expressly the concept of flagging dependent data loads recited in claim 9. However, Au discloses the flagging concept that is used to reject claim 9.

Peir et al. and Au are analogous art because they are from the same field of endeavor of determining and processing data/instructions that are dependent on other data/instructions.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify Peir et al. by including the step of setting a flag bit as taught by Au in column 8, at lines 44-46.

The motivation for doing so would have been to "maintain all command dependencies in a graph structure to reduce the number of address overlap-checks required" as expressly taught by Au in column 7, at lines 14-15.

Therefore, it would have been obvious to combine Au with Peir et al. for the benefit of command dependency indication to obtain the invention as specified in claim 11.

11. As per **claim 12**, Peir et al. and Au disclose the method recited in claim 9.

Au discloses, **"The D_flag field 308 is a bistate field" in column 7, at lines 46-47**, wherein the "bistate" is represented by a bit. In **Figure 3**, the "D_Flag" field 308

within "Command Record" 202. Record 202 corresponds to the "data load" from the claim.

12. As per **claim 13**, Peir et al. and Au disclose the method recited in claim 9.

Au discloses, in **Figure 3,** the "D_Flag" field 308 attached to the "Logical Block Address" 302 and 304. The "Logical Block Addresses" correspond to the "data load" from the claim. In addition, examiner notes that mere separation of parts (i.e. flags and data load) is not a patentable distinction over the prior art. See MPEP 2144.04 (C).

13. As per **claim 14**, the limitation "the step of flushing the flagged dependent specific data load from the pipeline upon the determination of a misprediction of a data load" is disclosed.

Peir et al. discloses **"A cache miss is detected during the regular cache access, all of the instructions that are scheduled during the speculative window may be canceled" in paragraph 18 and in Figure 3 (330).** The "flushing" from the claim corresponds to the instruction cancellation, and the "misprediction" from the claim corresponds to the "cache miss".

Peir et al. does not disclose expressly the limitation "flagged dependent specific data load".

Au discloses **"The D_Flag fields 308 in each record 202 indicate dependency relative to a more forward command record 202" in Figure 3 and in column 8, at lines 44-46.**

Peir et al. and Au are analogous art because they are from the same field of endeavor of determining and processing data/instructions that are dependent on other data/instructions.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify Peir et al. by including the step of setting a flag bit as taught by Au in column 8, at lines 44-46.

The motivation for doing so would have been to "maintain all command dependencies in a graph structure to reduce the number of address overlap-checks required" as expressly taught by Au in column 7, at lines 14-15.

Therefore, it would have been obvious to combine Au with Peir et al. for the benefit of command dependency indication to obtain the invention as specified in claim 14.

14. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Peir et al. and Au as applied to claim 1 above, and further in view of "The Cache Memory Book" by Jim Handy.

15. As per **claim 7**, Peir et al. and Au disclose the system recited in claim 1. However, Peir et al. and Au do not disclose expressly the limitation "the fast-load data cache includes a directory".

In paragraph 27 of the Applicant's specification, it is disclosed that a directory can be omitted if the cache is a one-way associate or direct-map cache. **Handy discloses a two-way associative cache in Page 54, at lines 23-25.** Since the cache is not a one-way associate or direct-map cache, it inherently includes a directory.

Peir et al., Au and Handy are analogous art because they are from the same field of endeavor of computer storage access/management.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify Peir et al. and Au by including the two-way associative cache as taught by Handy in Page 54.

The motivation for doing so would have been the high hit rate of the small size two-way associative cache as expressly taught by Handy in Page 55, Figure 2.9.

Therefore, it would have been obvious to combine Peir et al. and Au with Handy for the benefit of high cache hit rate to obtain the invention as specified in claim 7.

16. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Peir et al. and Au as applied to claim 1 above, and further in view of "The Cache Memory Book" by Jim Handy.

17. As per **claim 8**, Peir et al. and Au disclose the system recited in claim 1. However, Peir et al. and Au do not expressly disclose the limitation "the fast-load data cache does not include a directory."

Sato et al. discloses **"A set of routines which are frequently used in an OS is stored in a local memory arranged in a CPU and having high-speed elements" in column 2, at lines 23-26,** wherein the "local memory" corresponds to the "fast-load data cache" from the claim. Sato et al. also discloses **"A local memory which has part of address locations of the main memory as its address location, which is accessed by a CPU, and which can obtain same effect as cache memory without having cache directory" in the Abstract.**

Peir et al., Au and Sato et al. are analogous art because they are from the same field of endeavor of computer storage access/management.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify Peir et al. and Au by including the high-speed "local memory" without cache directory as taught by Sato et al. in column 2, at lines 23-26 and in the Abstract.

The motivation for doing so would have been the improved bus performance as expressly taught by Sato et al. in column 2, at lines 27-30.

Therefore, it would have been obvious to combine Peir et al. and Au with Handy for the benefit of improved bus performance to obtain the invention as specified in claim 8.

Relevant Art Cited by the Examiner

The following prior art made of record and not relied upon is cited to establish the level of skill in the applicant's art and those arts considered reasonably pertinent to applicant's disclosure. See MPEP 707.05(C).

The following reference teaches a pipelined system that minimizes the impact of a cache miss.

U.S. Patent Number	**Figures**
5,535,360	1

Conclusion

1. Claims Rejected in the Application

Per the instant office action, claims 1-16 have received a first action on the merits and are subject of a first action non-final.

2. Direction of Future Correspondences

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jae U. Yu whose telephone number is 571-272-1133. The examiner can normally be reached on M-F 9AM-5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald A. Sparks can be reached on 571-272-4201. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

January 11, 2006

Jae Un Yu
Patent Examiner
Art Unit 2185

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DONALD SPARKS
SUPERVISORY PATENT EXAMINER